--ABSTRACT

A bus system is provided which combines a number of internal lines, and leads them as a bundle to terminals. The internal lines are positioned within a processing unit having a multi-dimensional cell architecture.--

In the Claims:

Please delete "Patent claims" and in its place insert --WHAT IS CLAIMED IS:--.

Please cancel original claims 1-18, without prejudice.

Please add the following new claims:

--19. (New) A bus system, comprising:

a processing unit, the processing unit having a multi-dimensional programmable cell architecture; and

a first plurality of individual lines positioned within the processing unit, the first plurality of individual lines being bundled;

wherein the first plurality of individual lines provide a means to communicate between the processing unit and at least one of: i) an additional processing unit, ii) a memory device, and iii) a peripheral device.

20. (New) The bus system of claim 19, further comprising:

at least one interface unit coupled to the plurality of individual lines, the at least one interface unit combining the plurality of individual lines to form the bus system.